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Patent
Attorney's Docket No. 026350-028

#18 Reply Brief 12/4/02 ARJ

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	)	
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Toshiro HIRAMOTO et al.	)	Group Art Unit: 2826
	)	
Application No.: 09/389,321	)	Examiner: T. Dickey
	)	
Filed: September 3, 1999	)	Confirmation No.: 5290
	)	
For: MOS TRANSISTOR WITH A CONTROLLED THRESHOLD VOLTAGE	)	

REPLY BRIEF

Assistant Commissioner for Patents
Washington, D.C. 20231

Date: November 25, 2002

Sir:

This Reply Brief is filed in response to the Examiner's Answer dated September 25, 2002 (Paper No. 17). Concurrently filed with this Reply Brief is a Request for Oral Hearing. Also attached is a copy of Figs. 4 and 5.

In the Examiner's Answer, the Examiner continues to misunderstand the invention and to incorrectly define what the Examiner considers to be a EIB-MOS. In particular, applicants will again attempt to explain to the Board the differences between the prior art and the present invention.

Applicants respectfully bring the Board's attention to the specification at page 1, line 21 through page 2, line 11, page 3, lines 11-18, page 4, lines 6-12 and line 25 through page 6, line 6, page 8, line 17 through page 9, line 28. Attached to this Reply Brief is a copy of Figures 4 and 5 for the Board's convenience.

Threshold voltage of a MOS transistor is important for fast operation and power consumption. Normally, the threshold voltage of a transistor is constant while the transistor is turned on and off. However, it is possible to control the threshold voltage by changing a substrate voltage of a MOS transistor. A change in the threshold voltage is proportional to γ, which is a body effect factor of the MOS transistor. The threshold voltage of a VTMOS (variable threshold MOS) transistor is controlled by applying a first voltage to the substrate of the VTMOS transistor in an active mode and by applying a second smaller voltage than the first voltage to the substrate in a standby mode. Thus, the threshold voltage of the VTMOS will rise.

In order to control the threshold voltage effectively, it is preferable to make the body effect factor γ high. The body effect factor γ of a fully depleted SOI MOS transistor shown in Figure 4 is a function of the thickness of the gate oxide 19 divided by the sum of the thickness of the insulating layer 18 and the thickness of the single crystal layer 17 (i.e. $\gamma \fallingdotseq 3t_{fox2}/(3t_{fox} + t_{SOI1})$. In other words, the body effect factor is inversely proportional to the sum of the thickness of the single crystal layer 17 and the thickness of the insulating layer 18 (i.e. the depth of the depletion layer).

Therefore, one way to control the threshold voltage is to control the body effect factor γ. In other words, by changing the depth of the depletion layer, the threshold voltage of the transistor is controlled since the threshold voltage is proportional to the body effect factor γ.

In particular, as claimed in claims 1-12 of the present invention, by inducing a charge over the composition surface of the surrounded or body region, the depth of the

depletion layer is changed. Thus as shown in Figure 5, by inducing charges over the composition surface of the body or surrounded region,(i.e., the circles with the plus sign shown in body 26 of Figure 5), the body effect factor is approximately equal to the thickness of the gate oxide 28 divided by the thickness of the single crystal layer 21 (i.e. $\gamma \fallingdotseq 3t_{fox2}/t_{SOI2}$). Thus, the depth of the depletion layer is smaller in Figure 5 than the depth of the depletion layer of the fully depleted SOI MOS shown in Figure 4 (i.e., depth of depletion layer in Figure 5 is approximately equal to t_{SOI2} while the depth of the depletion layer in Figure 4 is equal to $t_{SOI1} + t_{box}$). In other words, due to inducing charge over the composition surface of the body region in Figure 5, the depth of the depletion layer decreases, which in turn increases the body effect factor. Thus, since the body effect factor γ is proportional to the threshold voltage, by increasing the body effect factor, the threshold voltage of the transistor will increase. Hence, in the present invention, by controlling inducing the charge over the composition surface of the surrounded or body region, the body effect factor will change and hence the threshold voltage of the transistor can be controlled.

In particular, the novel and unique feature of the invention claimed in claims 1-12 is that a p-type neutral region (i.e. holes) is induced in the body 26 by applying a voltage to the substrate. On the other hand, in a fully depleted SOI MOS transistor, the composition surface is depleted such that holes do not occur even though a voltage is applied (which is why it is called a fully depleted SOI MOS). The reason that holes cannot be introduced in the fully depleted SOI MOS is because no carriers exist within the body since the body is fully depleted.

Burr et al merely discloses a fully depleted SOI device. Therefore, when voltage is applied to the substrate of the SOI transistor of *Burr et al*, the voltage does not induce any charge over the composition surface of the body region since the SOI device of *Burr et al* is fully depleted. In other words, since the body region is fully depleted, no charge will occur because the composition surface is depleted and holes do not occur even though a voltage is applied.

Thus, applicants respectfully traverse the Examiner's Answer statement that "VTMOS is an EIB-MOS where the substrate voltage bias may be switched from a first voltage to a second, lower bias Application at page 2, lines 7-11." As explained above, a VTMOS is a fully depleted SOI MOS transistor and thus even though the substrate voltage bias may be switched between first and second voltages, no holes or a p-type neutral region is induced by the substrate voltage since the body of a VTMOS is fully depleted. In other words, in an EIB-MOS the p-region (i.e., holes) is induced under the body 26 electrically by the voltage applied to the substrate. A VTMOS is **not** a EIB-MOS.

Similarly, the Examiner's statement that "EIB-MOS appear to refer to a SOI MOS adapted for biasing the voltage of the substrate relative to the body" is similarly incorrect. As explained above, EIB (electrically induced body) refers to electrically inducing charge into a body as explained on page 9, lines 7-11 of the specification. In particular, the p-type neutral region (i.e., holes), which are not present in a conventional fully depleted SOI MOS transistor, is provided in the body 26 electrically by the voltage V_{SUB}. Thus as clearly stated on page 9, lines 7-11, a conventionally fully depleted SOI MOS transistor

does not (and will not) have a p-type neutral region (i.e., holes) provided in the body 26 when voltage is applied to the substrate.

Applicants also respectfully traverse the Examiner's statement that applicants' statements are particular theories concerning the physics of the device and do not define structure. Applicants respectfully submit that the Examiner does not recognize the importance and unique and novel features of the present invention in which there is a structure with a property of introducing holes into the body 26 by applying a voltage to the substrate 20.

On the other hand, the composition surface in *Burr et al* is depleted and holes do not occur although a substrate voltage is applied. Nowhere in *Burr et al* is it shown, taught or suggested to induce charges over a composition surface of the body or surrounded region.

Applicants respectfully point out that in *Burr et al* the voltage is applied to the substrate in order to control the threshold voltage. However, in the present invention, the voltage that is applied to the substrate is not to control the threshold voltage, but to introduce holes into the composition surface. By introducing the holes into the composition surface, the depth of the depletion layer is changed. Thus, the threshold voltage is controlled since the body effect factor γ is changed.

For all of the above stated reasons, it is respectfully requested that the Honorable Board of Patent Appeals and Interferences reverses the Examiner's decision in this case, since it is respectfully submitted that the final rejection of claims 1-12 is in error.

In the event that this paper is not timely filed within the currently set shortened statutory period, applicants respectfully petition for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

BURNS, DOANE, SWECKER & MATHIS, L.L.P.

By: _____
Ellen Marcie Emas
Registration No. 32,131

P.O. Box 1404
Alexandria, Virginia 22313-1404
(703) 836-6620

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FIG. 3
PRIOR ART

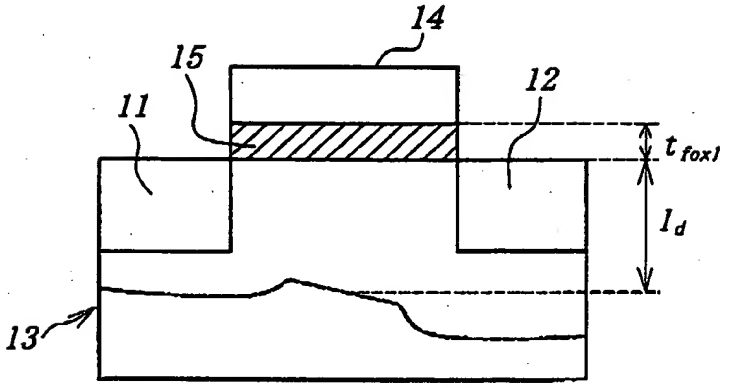

FIG. 4
PRIOR ART

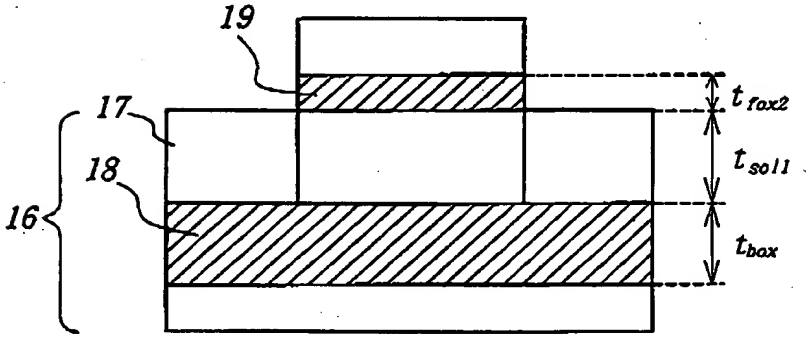

FIG. 5

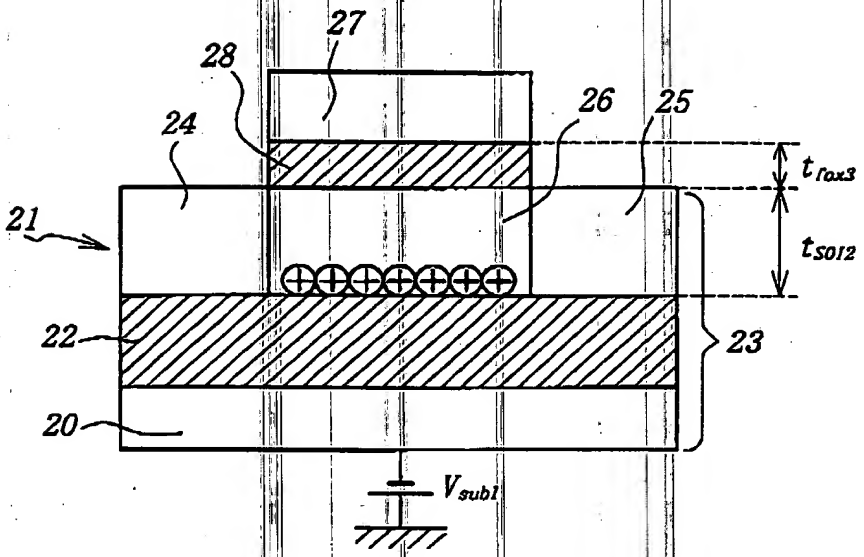

FIG. 6